JP,2570523,B

CLAIMS

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(57) [Claim(s)]

[Claim 1] The 1st and 2nd transistors by which both :drain electrodes were connected to the 1st power source in the current detector using two or more FET transistors, and both gate electrodes were connected to the input signal terminal;
Constant current source connected between the source electrode of said 1st transistor, and the 2nd power source;
Electrical-potential-difference comparator by which one input was connected to the source electrode of said 1st transistor, and the input of another side was connected to the source electrode and output terminal of said 2nd transistor;
The current detector characterized by detecting stably an excess of a predetermined value of the output current which flows said output terminal by comparing the potential of a preparation and the source electrode of said 2nd transistor with the potential of the source electrode of said 1st transistor.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to a current detector. It is the circuit which used power metal-oxide semiconductor field effect transistor for the detail more, and is related with the highly precise current detector which detects that the output current exceeded the maximum allowed value, and intercepts MOSFET.

[0002]

[Description of the Prior Art] Conventionally, there was a circuit as shown in drawing 1 as a current detector the voltage regulator using power metal-oxide semiconductor field effect transistor, and for Motor Driver. two juxtaposition n channel MOS FET transistors M1 which made the current detector 10 in the monolithic device as shown in this drawing, and M2 from -- it changes. MOSFET transistor M1 for detection which is the 1st transistor A drain electrode is the output current (load current) Io. Output terminal Po to receive Connecting, a gate electrode is the input signal terminal Vg. Connecting, a source electrode is the monitor resistance Rm. It minds and connects with the ground. Power-metal-oxide-semiconductor-field-effect-transistor transistor M2 which is the 2nd transistor Transistor M1 A drain electrode is an output terminal Po similarly. It connects and a gate electrode is the input signal terminal Vg. It connects. Transistor M2 The source electrode is directly connected to the ground. Thus, the output current Io By dividing into the power section and a detecting element, it is the monitor resistance Rm.

It carries out to detection and has come to be able to carry out insertion use. The current detector 10 has the electrical-potential-difference comparator COMP again. The non-inversed input terminal of the electrical-potential-difference comparator COMP is the 1st transistor M1. A source electrode and monitor resistance Rm The node of a between to electrical potential difference Vm It inputs. The inversed input terminal of the electrical-potential-difference comparator COMP inputs reference voltage Vrf from the positive electrode of the source of reference voltage where the negative electrode was grounded.
[0003] Below, actuation of the current detector 10 is explained. Generally, it is the drain current Id of MOSFET. Vds is expressed with a degree type in approximation in a very small active region compared with Vgs.
[0004] Id =K-W/L -(Vgs-Vth) Vds -- for a proportionality constant and W/L, the width versus length of a channel and Vgs are [K / threshold voltage and Vds of the electrical potential difference between the gate sources and Vth] the electrical potential differences between the drain sources here.
[0005] Monitor resistance Rm When it assumes that a value is sufficiently small, it is a transistor M1. Current I1 which flows when it is ON Rm to depend The value for a voltage drop Vm (= I1 and Rm) is a transistor M1. It can ignore compared with ON state voltage Vds between the drain sources. When this condition is fulfilled, it sets at an upper ceremony and is both the FET transistor M1 and M2. It can consider that Vds(es) and Vgs(es) are equal respectively. Since it can consider that both the transistors M1 and the threshold voltage Vth of M2 are almost equal, it is the FET transistor M2. Drain current I2 FET transistor M1 Drain current I1 A ratio I2 / I1 It is set to I2 / I1 =(W2 / L2)/(W1 / L1) =n, and becomes fixed. Therefore, it is I1 if mirror ratio n is known. By detecting a value, the value of I2 (= n-I1), therefore Io (= (n+1) and I1) can be known. It is good as a value of n at 1000.
[0006] Io I1 I1 since it can consider that it is in proportionality Monitor resistance Rm to depend A part for a voltage drop Vm It compares with reference voltage Vrf (refer to drawing 2), and is Vm. By detecting having exceeded reference voltage Vrf, it is Io. It is detectable to have exceeded the predetermined value. In the current detector 10 of drawing 1 , it is Vm. If reference voltage Vrf is exceeded, Comparator COMP is the current-limiting signal Co. It outputs (refer to drawing 2). Current-limiting signal Co By being outputted, it is the output current Io. It is detectable to have exceeded the predetermined value. Current-limiting signal Co For example, gate voltage Vg By inputting in the current-limiting circuit (not shown) to control, it is gate voltage Vg. It can be made zero and the MOSFET transistor M1 and M2 can be intercepted.
[0007] as mentioned above, proper precision with the comparatively good division current which flows between MOSFETs by which on resistance was adjusted within the monolithic device -- **** -- since it is, the power-metal-oxide-semiconductor-field-effect-transistor current detector 10 enables measurement of the load current of a power equalization circuit etc. somewhat efficiently. Monitor resistance Rm It is Rm if it is 10 or less % of the on resistance of the detecting-element transistor M1. Current I1 which can be disregarded and is detected It becomes the output current / current mirror ratio, i.e., I2 / n, mostly.
[0008]
[Problem(s) to be Solved by the Invention] However, in fact, it is the detecting-element transistor M1 in order to suppress detection loss low. Channel width W1 Transistor M2

W2 It must compare and must design small (W1 <<W2). In that case, transistor M1 It compares with on resistance and is Rm. If it is made small to extent which can be disregarded, it is the resistance Rm for detection. It becomes inadequate [the generated electrical potential difference for detection] for usually driving the current-limiting circuit containing a comparator etc. Therefore, it cannot but stop using a to some extent big value for Rm, and is Rm. It becomes impossible to ignore. Then, the sum total resistance by the side of detection (mirror) swells up considerably, and there is a trouble that current mirror ratio will change. Namely, Rm If it cannot ignore, it is a transistor M1. M2 The electrical potential difference Vds between the drain sources becomes mutually equal less, current mirror ratio is out of order by this, and detection precision worsens.
[0009] This invention aims at offering the current detector where detection precision is high in view of the above troubles.
[0010] Other purposes of this invention are offering a current detector without detection loss, without using the output current in a monitor circuit.
[0011]
[Means for Solving the Problem] Current detector 30 using two or more FET transistors which can be set to this invention in order to attain the above-mentioned purpose: Both drain electrodes are connected to the 1st power source Vdd. Both gate electrodes are the input signal terminals Vg. The 1st and 2nd connected transistors M1, M2 **; The 1st transistor M1 Constant current source Irf connected between a source electrode and the 2nd power source (ground); one input -- the 1st transistor M1 It connects with a source electrode. The input of another side is the 2nd transistor M2. Electrical-potential-difference comparator COMP connected to the source electrode and the output terminal; It has. The 2nd transistor M2 The potential and the 1st transistor M1 of a source electrode The output current Io which flows an output terminal by comparing the potential of a source electrode It is characterized by detecting an excess of a predetermined value.
[0012]
[Function] In the current detector of this invention constituted as mentioned above Both transistors M1 and M2 Both the source potential V1 and V2 When exactly equal (V1 =V2), it is the ratio I2 of the drain current of both transistors / I1. It operates so that it may be set to I2 / I1 =(W2 / L2)/(W1 / L1) =n (mirror ratio). In order that I1 may take a predetermined value according to a constant current source Irf, it is output current Io =I2. It will be set to I2 >I1 and n if it flows exceeding the maximum allowed current value Imx. Then, V2 It falls and is V1 >V2. The comparator COMP which became and detected it is the current-limiting signal Co. It outputs.
[0013]
[Example] The example of this invention is explained with reference to a drawing below. Drawing 3 shows the configuration of the current detector which is one example of this invention. two juxtaposition n channel MOS FET transistors M1 which made the current detector 30 in the monolithic device as shown in this drawing, and M2 from -- it changes. A transistor M1 and M2 A p channel may be used by circuitry as shown in drawing 5 , and you may be MOSFET of other formats. MOSFET transistor M1 for detection which is the 1st transistor A drain electrode is connected to supply voltage Rhine Vdd, and a gate electrode is the input signal terminal Vg. It connects and the source electrode is connected to the ground which is the 2nd power source through the constant current source Irf. Power-metal-oxide-semiconductor-field-effect-transistor transistor M2 which

is the 2nd transistor Transistor M1 Similarly, a drain electrode is connected to supply voltage Rhine Vdd, and a gate electrode is the input signal terminal Vg. It connects. Transistor M2 A source electrode is the output current (load current) Io. Output terminal Po to take out It connects. Thus, it sets to this invention and is the output current Io. It is not dividing into the power section and a detecting element. Therefore, a detecting element affects an output side. The current detector 30 has the electrical-potential-difference comparator COMP again. The non-inversed input terminal of the electrical-potential-difference comparator COMP is the 1st transistor M1. The node between a source electrode and a constant current source Irf to electrical potential difference V1 It inputs. the inversed input terminal of the electrical-potential-difference comparator COMP -- output terminal Po from -- electrical potential difference V2 It inputs. The electrical-potential-difference comparator COMP is the current-limiting output signal Co, if the reversal input value becomes smaller than a noninverting input value. It outputs.
[0014] Below, actuation of the current detector 30 is explained. Because of explanation of operation, it is both the transistors M1 and M2. Both the source potential V1 and V2 It is assumed mutually that it is an equal (V1 =V2) thing. At this time, the electrical-potential-difference comparator COMP is the current-limiting signal Co. It does not output. Generally it is the drain current Id of MOSFET. Vds is expressed with a degree type like the above-shown in a very small active region compared with Vgs.
[0015] Id =K-W/L By the -(Vgs-Vth) Vds above-mentioned assumption (V1 =V2), it is both the transistors M1 and M2. Electrical-potential-difference Vds(es) between the drain sources and electrical-potential-difference Vgs(es) between the gate sources are equal respectively. Both the transistors M1 and M2 Since it can consider that threshold voltage Vth is almost equal, it is the FET transistor M2. Drain current I2 FET transistor M1 The ratio I2 with the drain current I1 / I1 It is set to I2 / I1 =(W2 / L2)/(W1 / L1) =n. Thus, it is I1 when it shall operate according to mirror ratio n. By getting to know a value, the value of I2 (=n-I1), therefore Io (=I2 =n-I1) can be known. It is good as a value of n at 1000.
[0016] Thus, both the source potential V1 and V2 It is Io when equal. I1 Proportionality changes and it is **********. However, it is I1 by the constant current source Irf in fact. A predetermined value is taken. The output current Io, i.e., I2, A maximum allowed current value is set to Imx, and the current value of a constant current source Irf is set up with Imx/n. By doing so, it is I2. It is I1 when it flows exceeding Imx. Since it is still Irf (=Imx/n), it is set to I2 >I1 and n. Then, I2 =n-I1 Proportionality collapses and it is V2. It falls and is V1 >V2. It becomes. The comparator COMP which detected it is the current-limiting signal Co. It outputs (refer to drawing 4). Therefore, current-limiting signal Co By having been outputted, it is Io. It is detectable to have exceeded Imx. Current-limiting signal Co For example, gate voltage Vg By outputting to the current-limiting circuit (not shown) to control, it is gate voltage Vg. It is made zero and is the MOSFET transistor M1 and M2. It can intercept.
[0017]
[Effect of the Invention] This invention is the monitor resistance Rm which was experienced with the conventional technique since it was constituted as above-mentioned. The detection error to depend is avoidable, it is a high precision and the effectiveness of enabling detection/limit of the load current efficiently is acquired. Moreover, current I1 for detection in a monitor circuit It is supplied from the constant current source Irf, and is

the output current Io. Since a part is not necessarily used, it is Io. It is not affected, but effectiveness and precision are easy also for the design of an at best still more suitable stabilization circuit, and there is great effectiveness -- it is hard to be influenced by the service condition of a circuit.

TECHNICAL FIELD

[Industrial Application] This invention relates to a current detector. It is the circuit which used power metal-oxide semiconductor field effect transistor for the detail more, and is related with the highly precise current detector which detects that the output current exceeded the maximum allowed value, and intercepts MOSFET.

PRIOR ART

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EFFECT OF THE INVENTION

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TECHNICAL PROBLEM

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OPERATION

[Function] In the current detector of this invention constituted as mentioned above Both transistors M1 and M2 Both the source potential V1 and V2 When exactly equal (V1 =V2), it is the ratio I2 of the drain current of both transistors / I1. It operates so that it may be set to I2 / I1 =(W2 / L2)/(W1 / L1) =n (mirror ratio). In order that I1 may take a predetermined value according to a constant current source Irf, it is output current Io =I2. It will be set to I2 >I1 and n if it flows exceeding the maximum allowed current value Imx. Then, V2 It falls and is V1 >V2. The comparator COMP which became and detected it is the current-limiting signal Co. It outputs.
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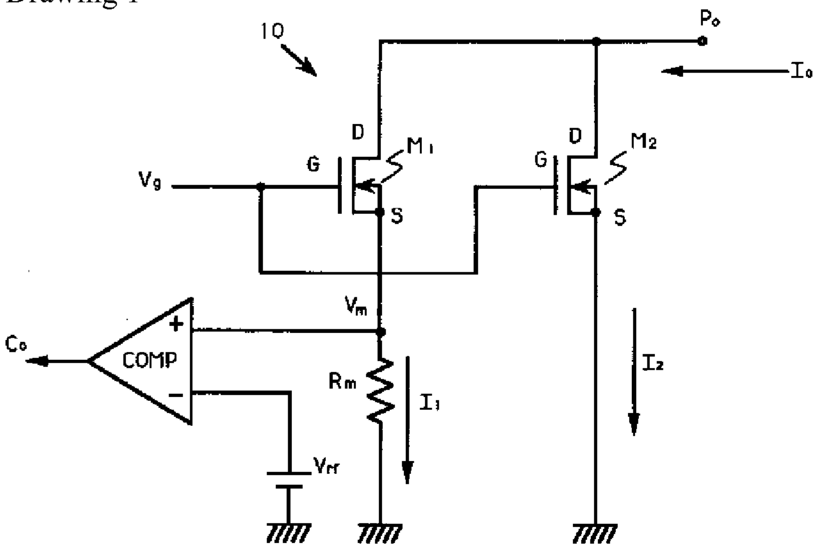
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The conventional current detector is shown.
[Drawing 2] It is a graph explaining actuation of the circuit of drawing 1 .
[Drawing 3] The current detector according to one example of this invention is shown.
[Drawing 4] It is a graph explaining actuation of the circuit of drawing 3 .
[Drawing 5] The current detector according to other examples of this invention is shown.
[Description of Notations]
30 Current Detector
Vdd Supply voltage

Vg Input signal electrical potential difference
M1 The 1st transistor
M2 The 2nd transistor
Irf Constant current source
Po Output terminal
COMP Electrical-potential-difference comparator
Io Output current

Drawing 1



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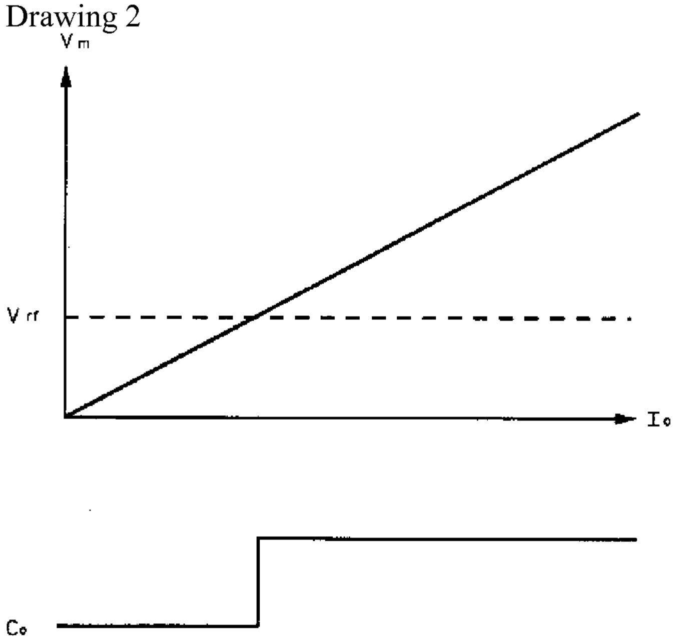

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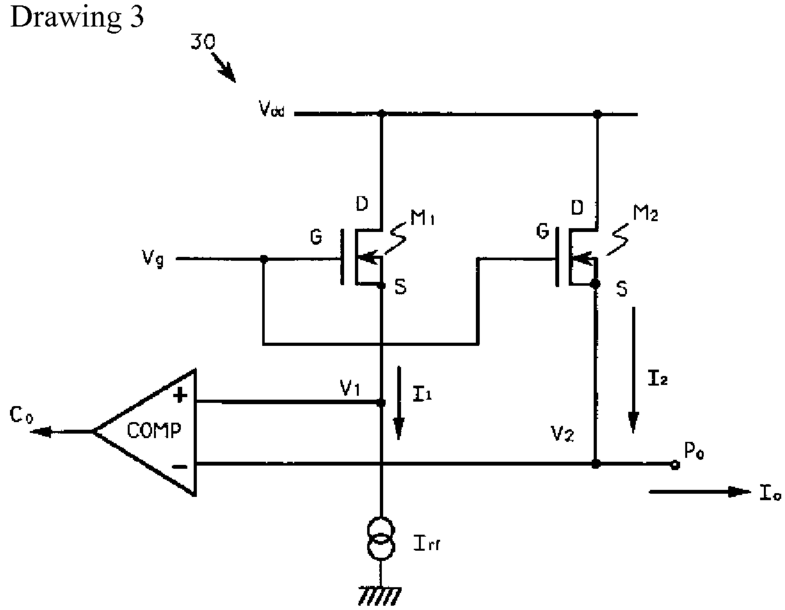

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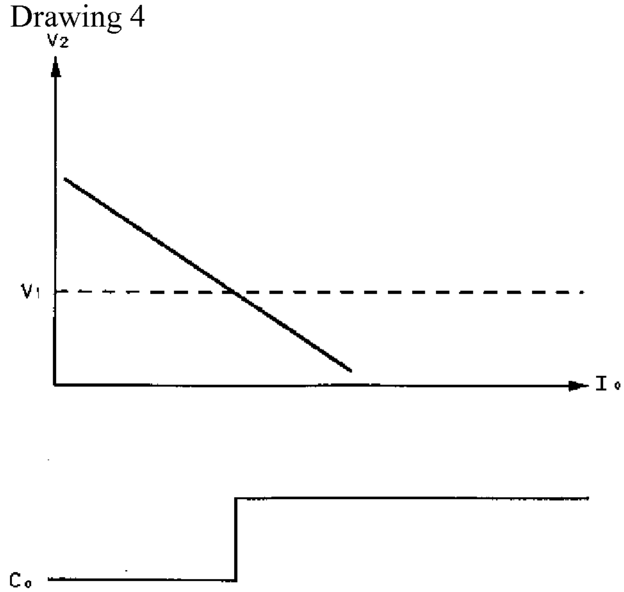
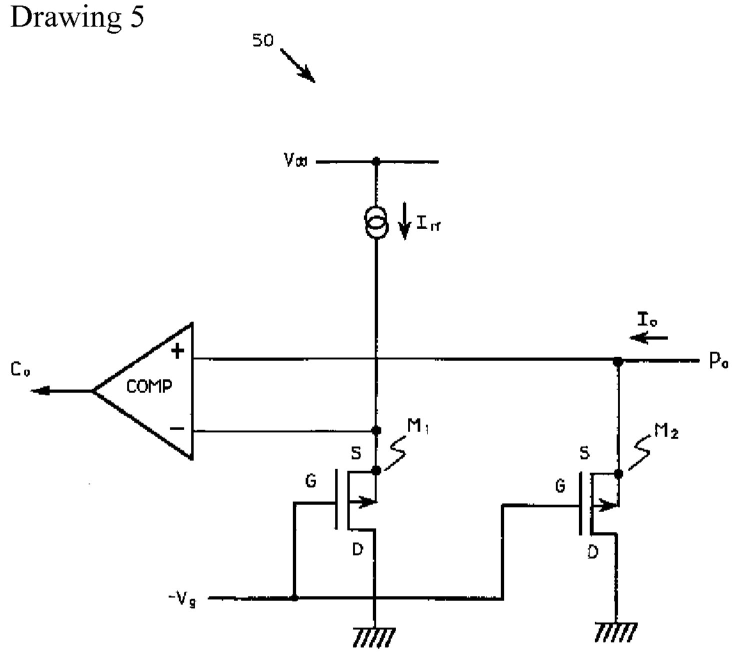


Drawing 5



(19)日本国特許庁（ＪＰ）　(12) 特　許　公　報（Ｂ２）　(11)特許番号

第2570523号

(45)発行日　平成９年(1997)１月８日　(24)登録日　平成８年(1996)10月24日

(51)Int.Cl.⁶		識別記号	庁内整理番号	ＦＩ		技術表示箇所
ＧＯ１Ｒ	19/165			ＧＯ１Ｒ	19/165	Ｌ
ＧＯ５Ｆ	1/10	３０４		ＧＯ５Ｆ	1/10	３０４Ｌ
	1/56	３１０			1/56	３１０Ｐ

請求項の数１（全　５　頁）

(21)出願番号　特願平3－235706

(22)出願日　平成３年(1991)８月23日

(65)公開番号　特開平5－52880

(43)公開日　平成５年(1993)３月２日

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(56)参考文献　特開　平３－75572（ＪＰ，Ａ）
特開　平３－186770（ＪＰ，Ａ）
特開　昭62－247268（ＪＰ，Ａ）

(54)【発明の名称】　電流検出回路

1

(57)【特許請求の範囲】

【請求項１】　複数個のＦＥＴトランジスタを用いた電流検出回路において：

ドレイン電極が共に第１電源に接続され、ゲート電極が共に入力信号端子に接続された第１および第２トランジスタと；

前記第１トランジスタのソース電極と第２電源との間に接続された定電流源と；

一方の入力が前記第１トランジスタのソース電極に接続され，他方の入力が前記第２トランジスタのソース電極および出力端子に接続された電圧比較器と；

を備え、

前記第２トランジスタのソース電極の電位と前記第１トランジスタのソース電極の電位とを比較することによって前記出力端子を流れる出力電流の所定値超過を安定的に検出することを特徴とする電流検出回路。

2

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、電流検出回路に関するものである。より詳細には，パワーＭＯＳＦＥＴを用いた回路であって，出力電流が最大許容値を越えたことを検出しＭＯＳＦＥＴを遮断する高精度の電流検出回路に関するものである。

【０００２】

【従来の技術】従来、パワーＭＯＳＦＥＴを用いた電源用ＩＣやモータドライバー用の電流検出回路として、図１に示すような回路があった。同図に示されるように、電流検出回路１０は、モノリシックデバイス内に作った２個の並列ｎチャネルＭＯＳＦＥＴトランジスタM_1、M_2 から成る。第１のトランジスタである検出用ＭＯＳ

ＦＥＴトランジスタM_1のドレイン電極は出力電流（負荷電流）I_oを受ける出力端子P_oに接続され、ゲート電極は入力信号端子V_gに接続され、ソース電極はモニター抵抗R_mを介してアースに接続されている。第２のトランジスタであるパワーＭＯＳＦＥＴトランジスタM_2は、トランジスタM_1と同様に、ドレイン電極が出力端子P_oに接続され、ゲート電極が入力信号端子V_gに接続されている。トランジスタM_2のソース電極はアースに直接に接続されている。このように出力電流I_oをパワー部と検出部とに分割することによって、モニター抵抗R_mを検出用として挿入使用できるようになっている。電流検出回路１０はまた、電圧比較器ＣＯＭＰを有する。電圧比較器ＣＯＭＰの非反転入力端子は、第１のトランジスタM_1のソース電極とモニター抵抗R_mとの間のノードから電圧V_mを入力する。電圧比較器ＣＯＭＰの反転入力端子は、負極がアースされた基準電圧源の正極から基準電圧V_{rf}を入力する。

【０００３】以下に、電流検出回路１０の動作について説明する。一般に、ＭＯＳＦＥＴのドレイン電流I_dは、V_{ds}がV_{gs}に比べて極めて小さい動作領域においては、近似的に次式で表される。

【０００４】$I_d = K \cdot W/L \cdot (V_{gs} - V_{th}) V_{ds}$

ここに、Ｋは比例定数、Ｗ／Ｌはチャネルの幅対長さ、V_{gs}はゲートソース間電圧、V_{th}は閾値電圧、V_{ds}はドレインソース間電圧である。

【０００５】モニター抵抗R_mの値が十分小さいと仮定すると、トランジスタM_1がオンのときに流れる電流I_1によるR_mの電圧降下分V_m（$= I_1 \cdot R_m$）の値が、トランジスタM_1のドレインソース間オン電圧V_{ds}に比べて無視できる。この条件が満たされていると、上式において、両ＦＥＴトランジスタM_1、M_2のV_{ds}どうしおよびV_{gs}どうしをそれぞれ等しいとみなせる。両トランジスタM_1、M_2の閾値電圧V_{th}はほぼ等しいとみなせるので、ＦＥＴトランジスタM_2のドレイン電流I_2とＦＥＴトランジスタM_1のドレイン電流I_1との比I_2/I_1が、$I_2/I_1 = (W_2/L_2)/(W_1/L_1) = n$となり、一定になる。したがってミラー比nが分かっていれば、I_1の値を検出することにより、I_2（$= n \cdot I_1$）の値、ゆえにI_o（$= (n+1) \cdot I_1$）を知ることができる。nの値としてたとえば1000で良い。

【０００６】I_oとI_1が比例関係にあるとみなせることから、I_1によるモニター抵抗R_mの電圧降下分V_mを基準電圧V_{rf}と比較し（図２参照）、V_mが基準電圧V_{rf}を越えたことを検出することによって、I_oが所定値を越えたことを検出することができる。図１の電流検出回路１０では、V_mが基準電圧V_{rf}を越えると、比較器ＣＯＭＰが電流制限信号C_oを出力する（図２参照）。電流制限信号C_oが出力されることにより、出力電流I_oが所定の値を越えたことを検出することができる。電流制限信号C_oをたとえばゲート電圧V_gを制御する電流制限回路（図示せず）内に入力することによって、ゲート電圧V_gをゼロにし、ＭＯＳＦＥＴトランジスタM_1、M_2を遮断することができる。

【０００７】上記のように、モノリシックデバイス内でオン抵抗が整合されたＭＯＳＦＥＴ間を流れる分割電流は比較的良好な固有精度をもっているので、パワーＭＯＳＦＥＴ電流検出回路１０は、ある程度効率良くパワー調整回路等の負荷電流の測定を可能にする。モニター抵抗R_mが検出部トランジスタM_1のオン抵抗の１０パーセント以下であれば、R_mを無視することができ、検出する電流I_1は、ほぼ出力電流／電流ミラー比、つまりI_2/nになる。

【０００８】

【発明が解決しようとする課題】しかしながら、実際には、検出損失を低く抑えるために検出部トランジスタM_1のチャネル幅W_1をトランジスタM_2のW_2に比べて小さく（$W_1 << W_2$）設計しなければならず、その場合にトランジスタM_1のオン抵抗に比べてR_mを無視できる程度に小さくすると、検出用抵抗R_mで発生した検出用電圧では通常、比較器等を含む電流制限回路をドライブするには不十分となる。従って、R_mにはある程度大きな値を使用せざるを得なくなり、R_mを無視できなくなる。すると、検出（ミラー）側の合計抵抗がかなり膨れ上がり、電流ミラー比が変わってしまうという問題点がある。すなわち、R_mを無視できないと、トランジスタM_1とM_2とのドレインソース間電圧V_{ds}が互いに等しくなくなってしまい、これにより電流ミラー比が狂ってしまい検出精度が悪くなる。

【０００９】本発明は、上記のような問題点に鑑み、検出精度の高い電流検出回路を提供することを目的としている。

【００１０】本発明の他の目的は、モニター回路において出力電流を利用せずに、検出損失のない電流検出回路を提供することである。

【００１１】

【課題を解決するための手段】上記目的を達成するために、本発明における複数個のＦＥＴトランジスタを用いた電流検出回路３０は；　ドレイン電極が共に第１電源V_{dd}に接続され、ゲート電極が共に入力信号端子V_gに接続された第１および第２トランジスタM_1、M_2と；

第１トランジスタM_1のソース電極と第２電源（アース）との間に接続された定電流源I_{rf}と；　一方の入力が第１トランジスタM_1のソース電極に接続され、他方の入力が第２トランジスタM_2のソース電極および出力端子に接続された電圧比較器ＣＯＭＰと；　を備え、

第２トランジスタM_2のソース電極の電位と第１トランジスタM_1のソース電極の電位とを比較することによって出力端子を流れる出力電流I_oの所定値超過を検出することを特徴とするものである。

【0012】
【作用】上記のように構成した本発明の電流検出回路においては、両トランジスタM_1、M_2の両ソース電位V_1、V_2がちょうど等しい（$V_1=V_2$）ときに、両トランジスタのドレイン電流の比I_2/I_1が、$I_2/I_1=(W_2/L_2)/(W_1/L_1)=n$（ミラー比）となるように動作する。定電流源$I_{rf}$により$I_1$は所定の値をとるため、出力電流$I_o=I_2$が最大許容電流値$I_{mx}$を越えて流れると、$I_2>I_1\cdot n$となる。すると$V_2$が低下し$V_1>V_2$となり、それを検出した比較器COMPが、電流制限信号C_oを出力する。

【0013】
【実施例】以下に本発明の実施例について図面を参照して説明する。図3は、本発明の一実施例である電流検出回路の構成を示す。同図に示されるように、電流検出回路30は、モノリシックデバイス内に作った2個の並列nチャネルMOSFETトランジスタM_1、M_2から成る。トランジスタM_1、M_2は、図5に示すような回路構成によりpチャネルを使用しても良く、他の形式のMOSFETであっても良い。第1のトランジスタである検出用MOSFETトランジスタM_1のドレイン電極は電源電圧ラインV_{dd}に接続され、ゲート電極は入力信号端子V_gに接続され、ソース電極は定電流源I_{rf}を介して第2電源であるアースに接続されている。第2のトランジスタであるパワーMOSFETトランジスタM_2は、トランジスタM_1と同様に、ドレイン電極が電源電圧ラインV_{dd}に接続され、ゲート電極が入力信号端子V_gに接続されている。トランジスタM_2のソース電極は出力電流（負荷電流）I_oを取り出す出力端子P_oに接続されている。このように本発明においては、出力電流I_oをパワー部と検出部とに分割していない。そのため、検出部が出力側に影響を及ぼさないようになっている。電流検出回路30はまた、電圧比較器COMPを有する。電圧比較器COMPの非反転入力端子は、第1のトランジスタM_1のソース電極と定電流源I_{rf}との間のノードから電圧V_1を入力する。電圧比較器COMPの反転入力端子は、出力端子P_oから電圧V_2を入力する。電圧比較器COMPは、その反転入力値が非反転入力値より小さくなると、電流制限出力信号C_oを出力する。

【0014】以下に、電流検出回路30の動作について説明する。動作の説明のために、両トランジスタM_1、M_2の両ソース電位V_1、V_2を互いに等しい（$V_1=V_2$）ものと仮定する。このとき、電圧比較器COMPは電流制限信号C_oを出力しない。一般にMOSFETのドレイン電流I_dは、V_{ds}がV_{gs}に比べて極めて小さい動作領域においては、前掲と同様に次式で表される。

【0015】$I_d=K\cdot W/L\cdot(V_{gs}-V_{th})V_{ds}$

上記仮定（$V_1=V_2$）により、両トランジスタM_1、M_2のドレインソース間電圧V_{ds}どうしおよびゲートソース間電圧V_{gs}どうしがそれぞれ等しい。両トランジスタM_1、M_2の閾値電圧V_{th}はほぼ等しいとみなせるので、FETトランジスタM_2のドレイン電流I_2とFETトランジスタM_1のドレイン電流I_1との比I_2/I_1は、$I_2/I_1=(W_2/L_2)/(W_1/L_1)=n$となる。このようにミラー比nにしたがって動作しているものとすると、I_1の値を知ることにより、I_2（$=n\cdot I_1$）の値、ゆえにI_o（$=I_2=n\cdot I_1$）を知ることができる。nの値としてたとえば1000で良い。

【0016】このように両ソース電位V_1、V_2が等しいときは、I_oとI_1の比例関係が成り立っている。ところが、実際には定電流源I_{rf}によりI_1は所定の値をとる。出力電流I_o、すなわちI_2の最大許容電流値をI_{mx}とし、定電流源I_{rf}の電流値をI_{mx}/nと設定しておく。そうすることにより、I_2がI_{mx}を越えて流れたとき、I_1はI_{rf}（$=I_{mx}/n$）のままであることから、$I_2>I_1\cdot n$となる。すると$I_2=n\cdot I_1$の比例関係が崩れ、V_2が低下し$V_1>V_2$となる。それを検出した比較器COMPが、電流制限信号C_oを出力する（図4参照）。したがって、電流制限信号C_oが出力されたことによって、I_oがI_{mx}を越えたことを検出することができる。電流制限信号C_oをたとえばゲート電圧V_gを制御する電流制限回路（図示せず）に出力することによって、ゲート電圧V_gをゼロにし、MOSFETトランジスタM_1、M_2を遮断することができる。

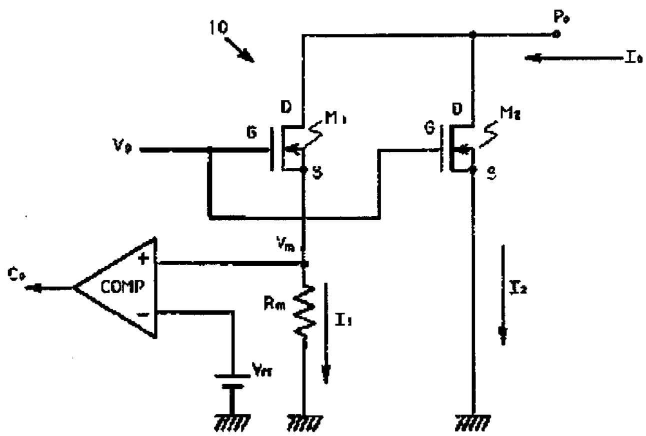
【0017】
【発明の効果】本発明は、上述のとおり構成されているので、従来技術で経験したようなモニター抵抗R_mによる検出誤差を回避することができ、高い精度でかつ効率良く負荷電流の検出／制限を可能にするという効果が得られる。また、モニター回路での検出用電流I_1は定電流源I_{rf}から供給されており、出力電流I_oの一部を利用するわけではないので、I_oに影響を与えず、効率・精度が良く、さらに適当な安定化回路の設計も容易であり回路の使用条件による影響も受けにくいなど、多大の効果がある。

【図面の簡単な説明】
【図1】従来の電流検出回路を示す。
【図2】図1の回路の動作を説明するグラフである。
【図3】本発明の一実施例にしたがった電流検出回路を示す。
【図4】図3の回路の動作を説明するグラフである。
【図5】本発明の他の実施例にしたがった電流検出回路を示す。

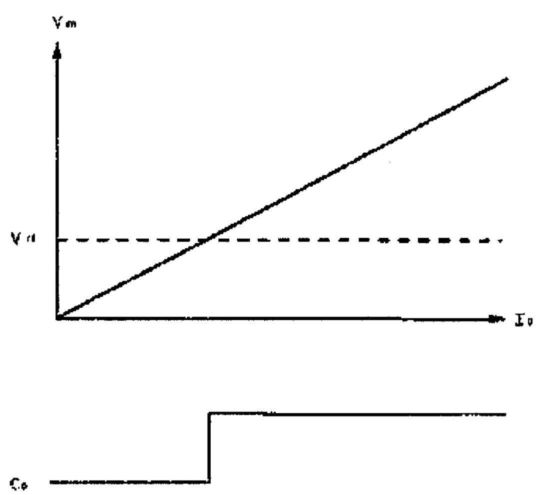
【符号の説明】
30　電流検出回路
V_{dd}　電源電圧
V_g　入力信号電圧
M_1　第1トランジスタ

M_2 第2トランジスタ
i_{rf} 定電流源
P_o 出力端子
＊COMP 電圧比較器
i_o 出力電流
＊

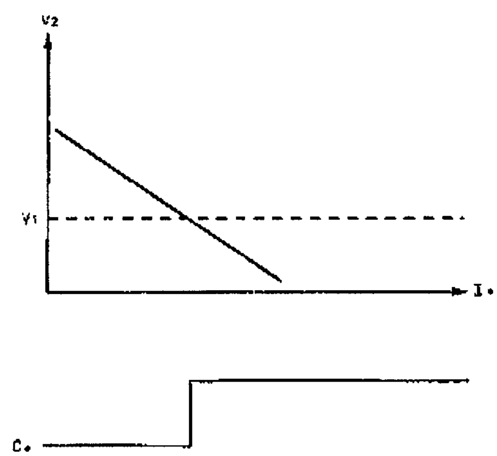
【図1】



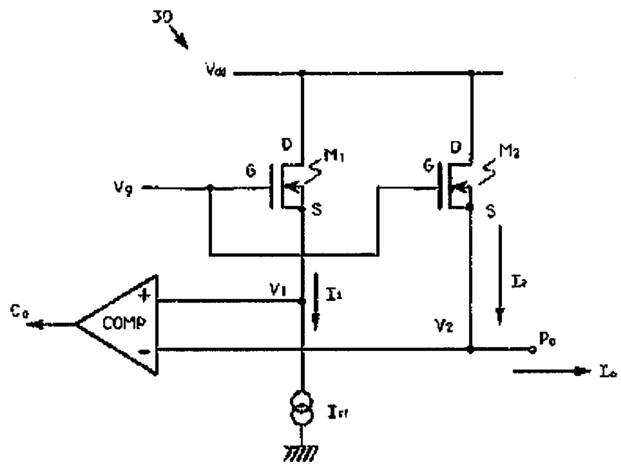
【図2】



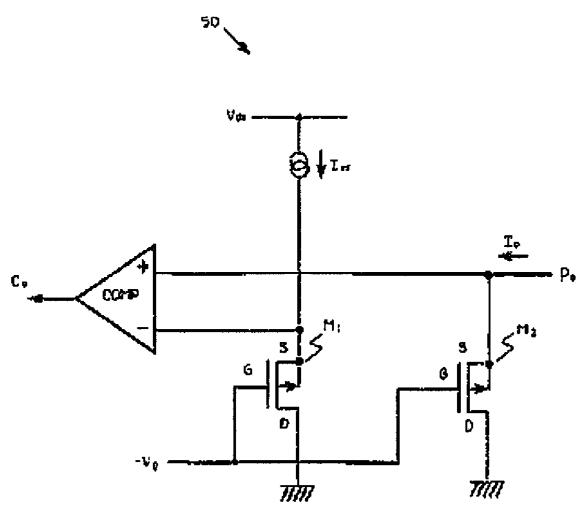
【図4】



【図３】


30
Vdd
D
M1
G
Vg
S
D
M2
G
S
I2
V1
I1
Co
COMP
+
-
V2
Po
Io
Iref

【図５】


50
Vdd
Iref
Io
Po
Co
COMP
+
-
M1
S
G
D
M2
S
G
D
-Vg